

FIG. 1
programmable
logic device 10

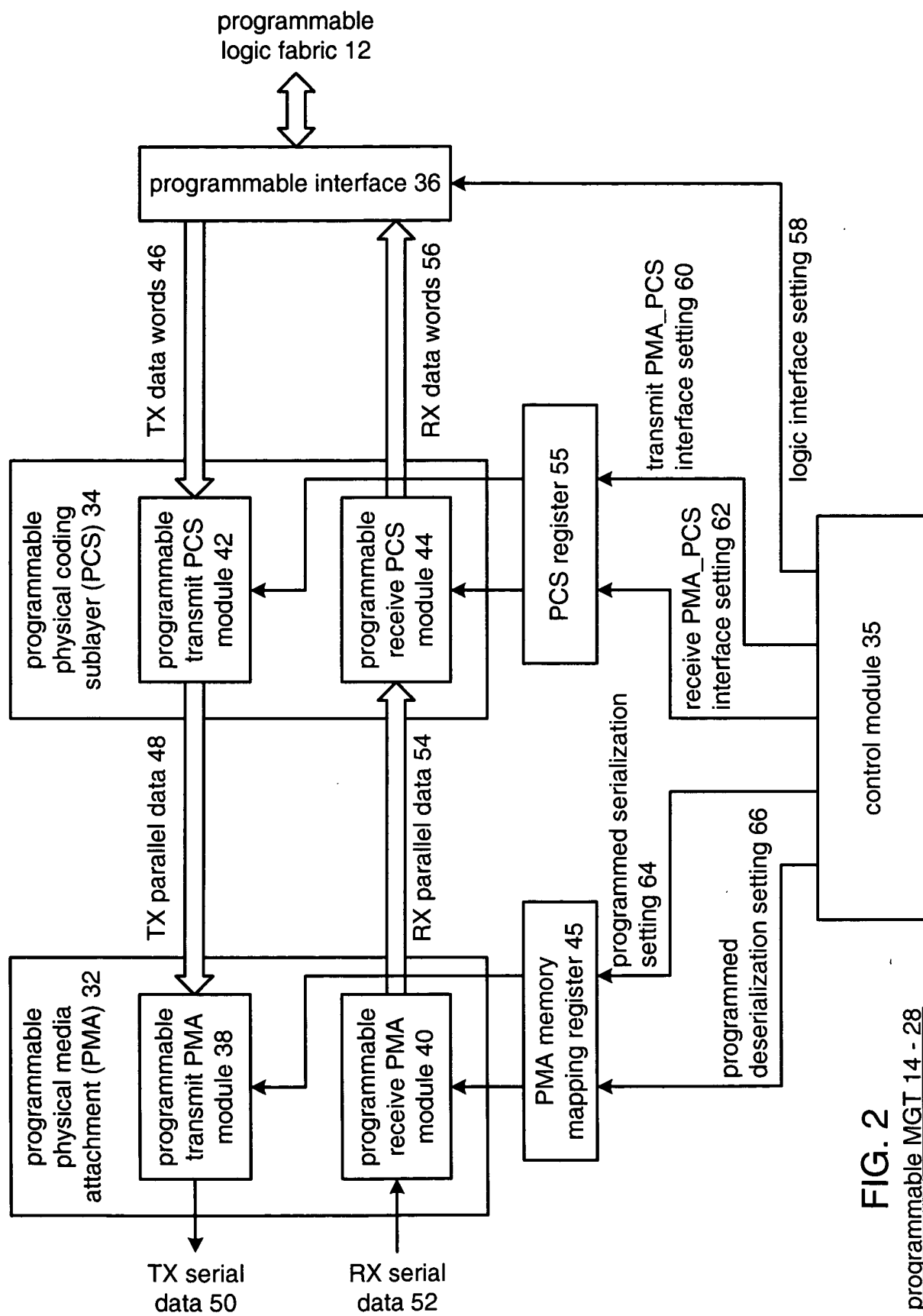


FIG. 2
programmable MGT 14 - 28

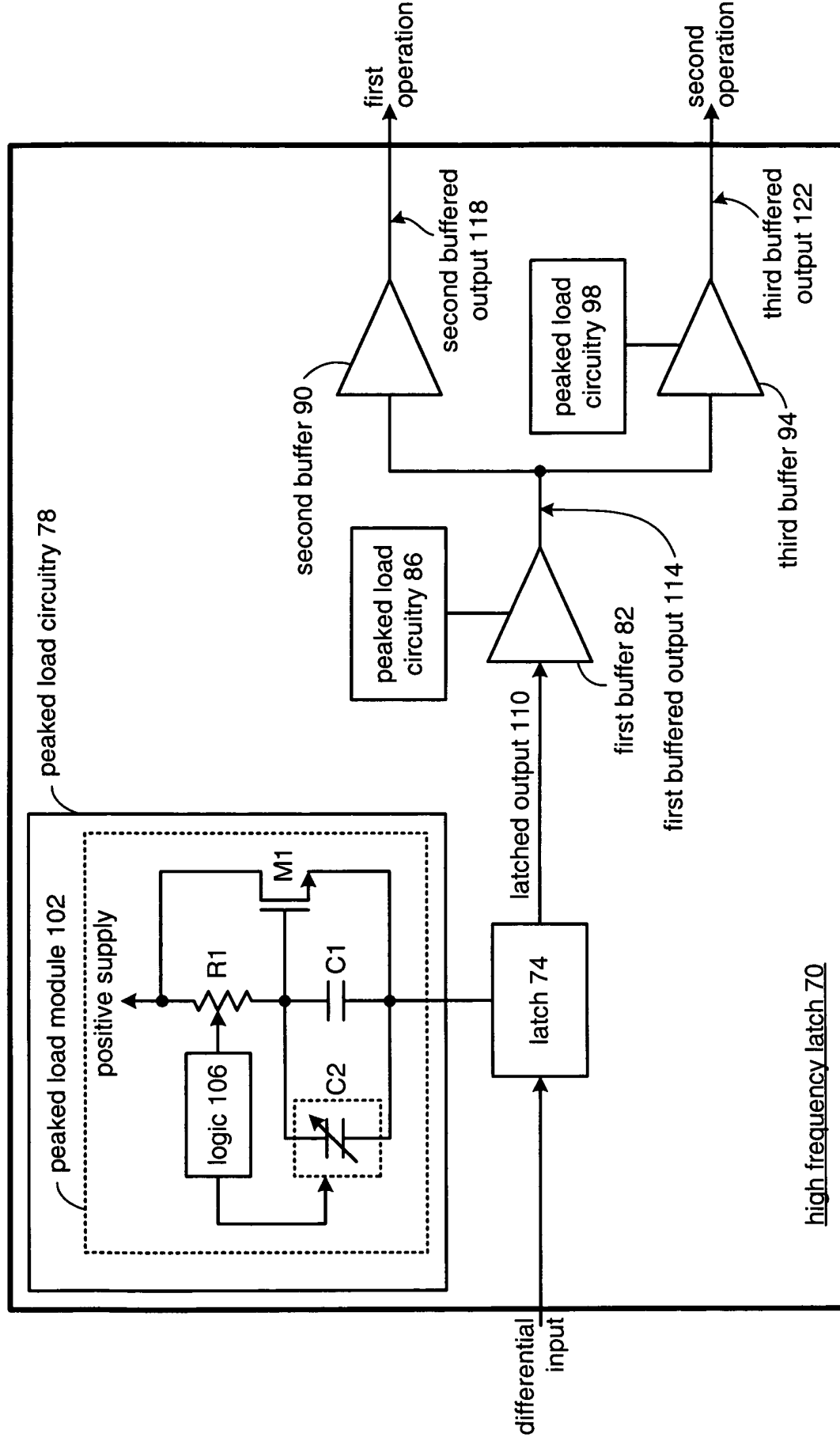


FIG. 3
high frequency latch 70

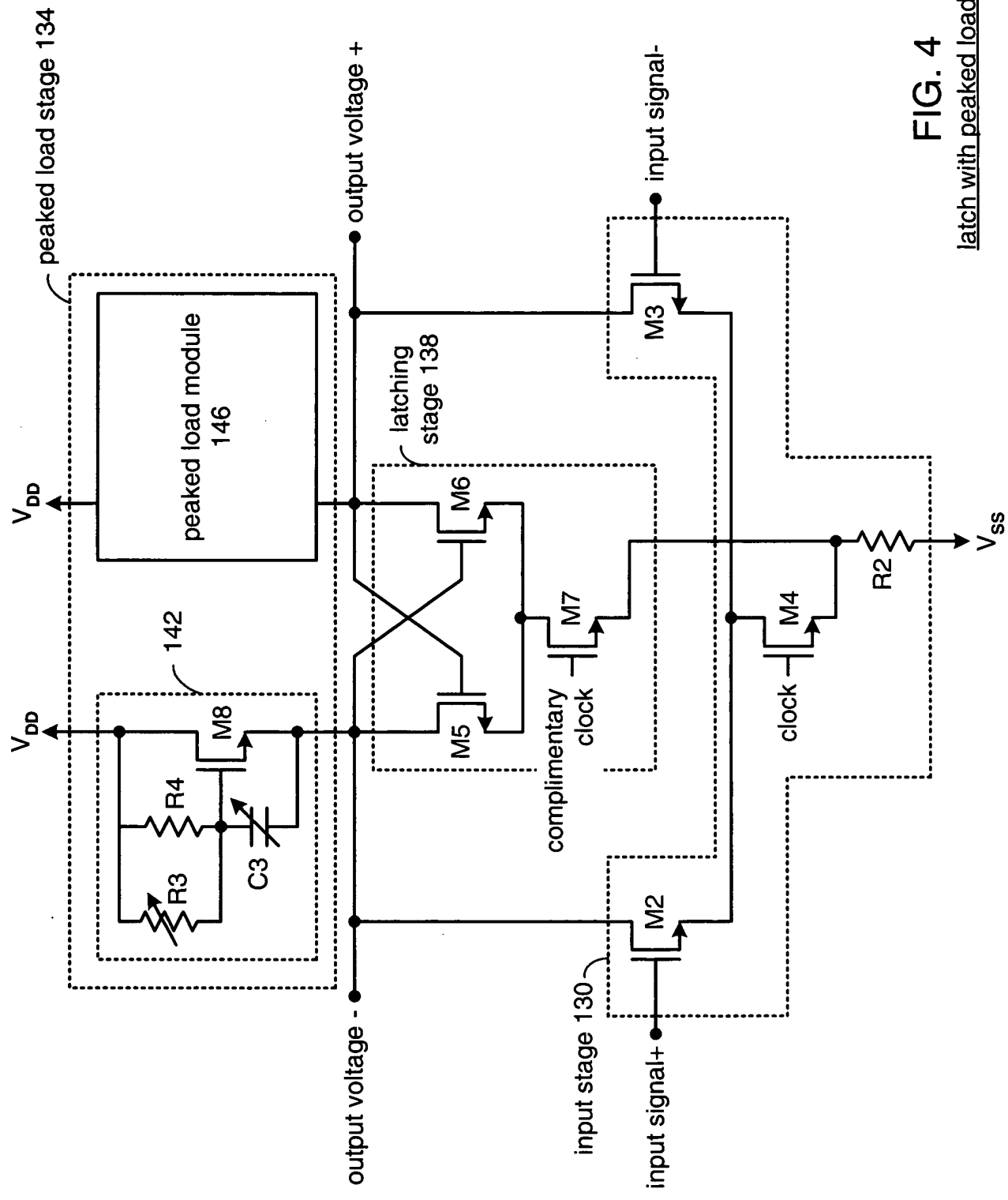


FIG. 4
latch with peaked load stage

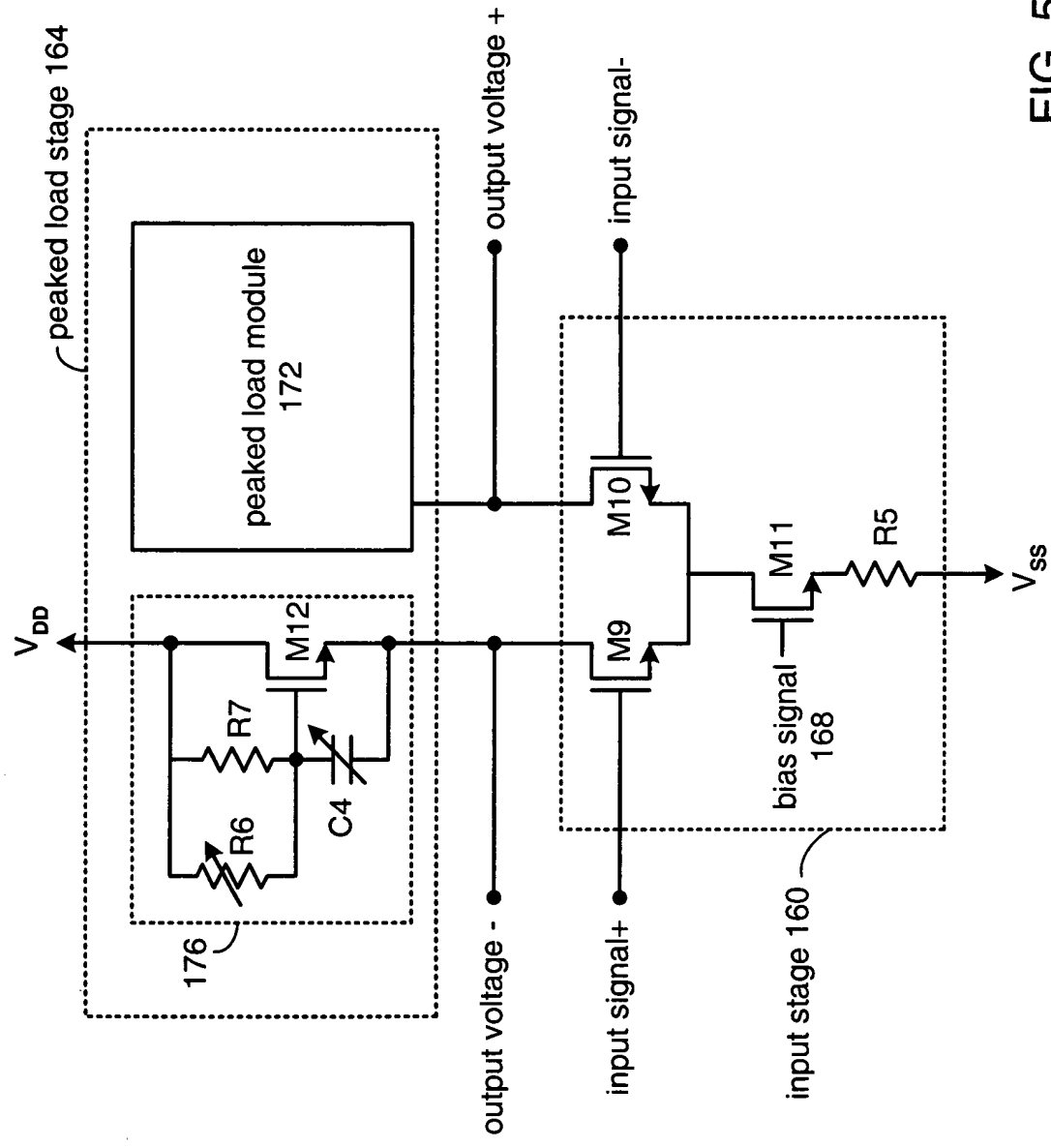


FIG. 5

buffer with peaked load stage

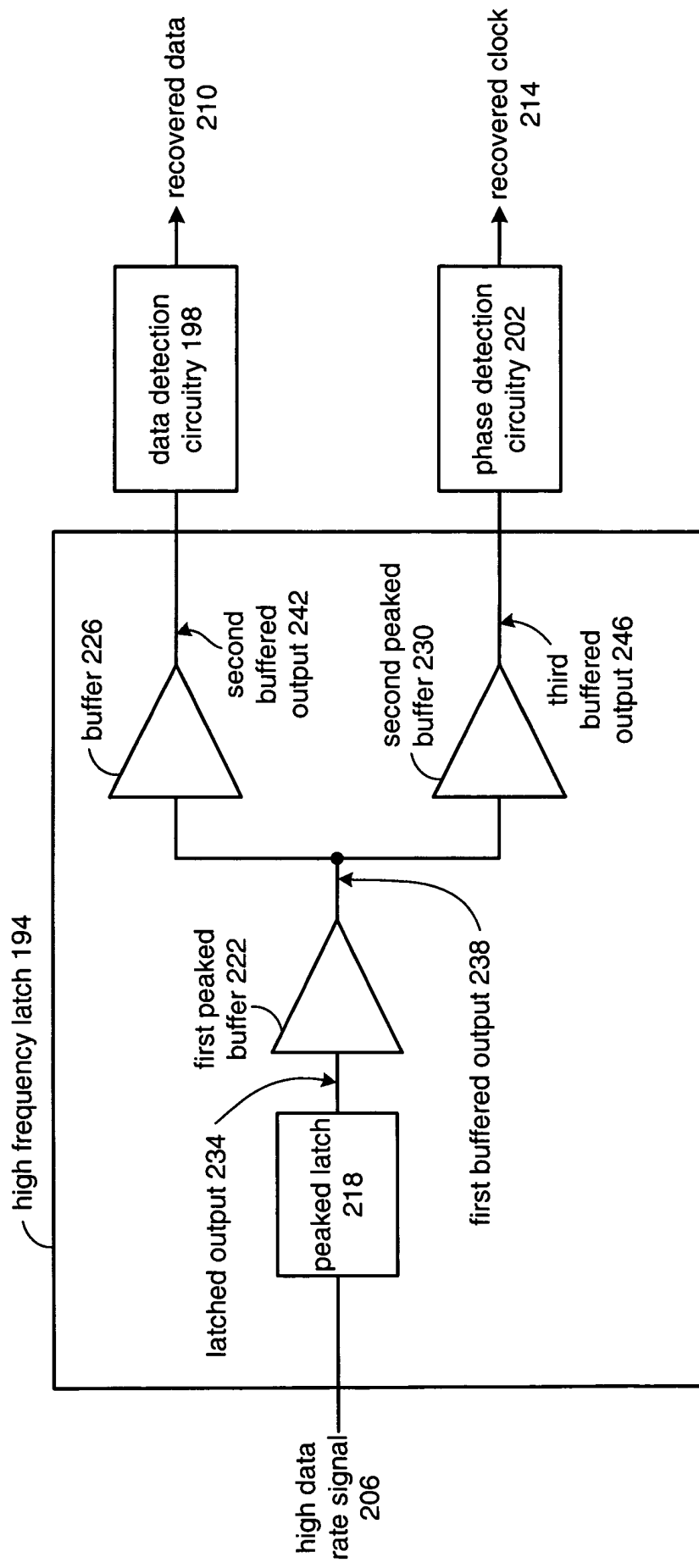


FIG. 6
clock and data recovery module 190

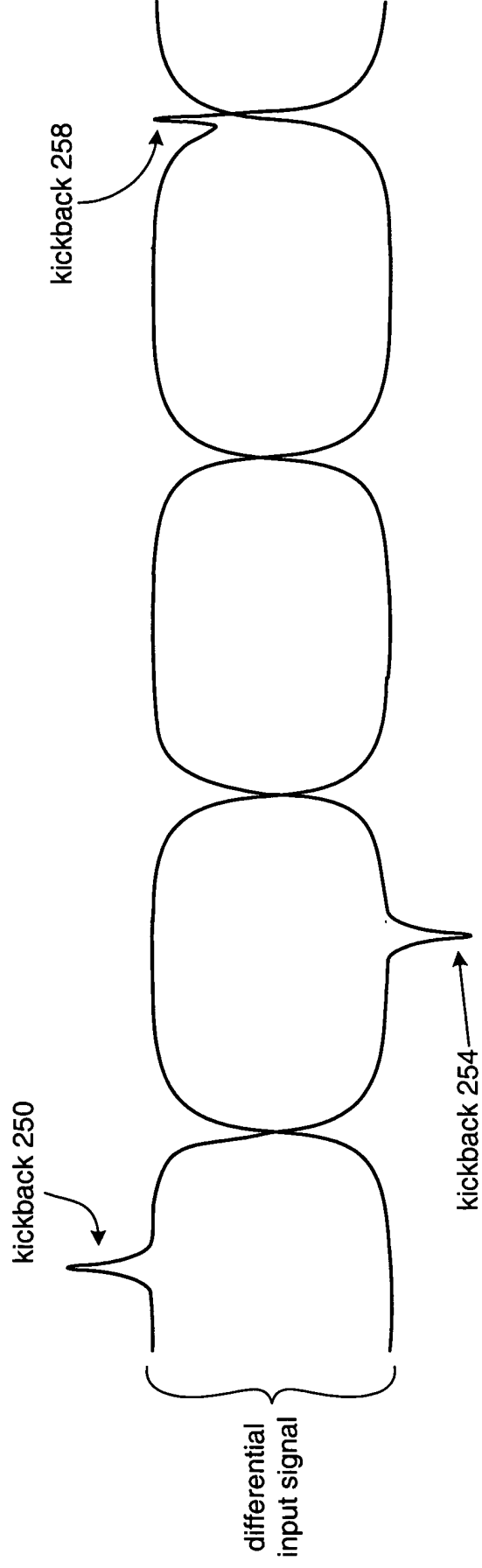


FIG. 7
differential signal with kickback

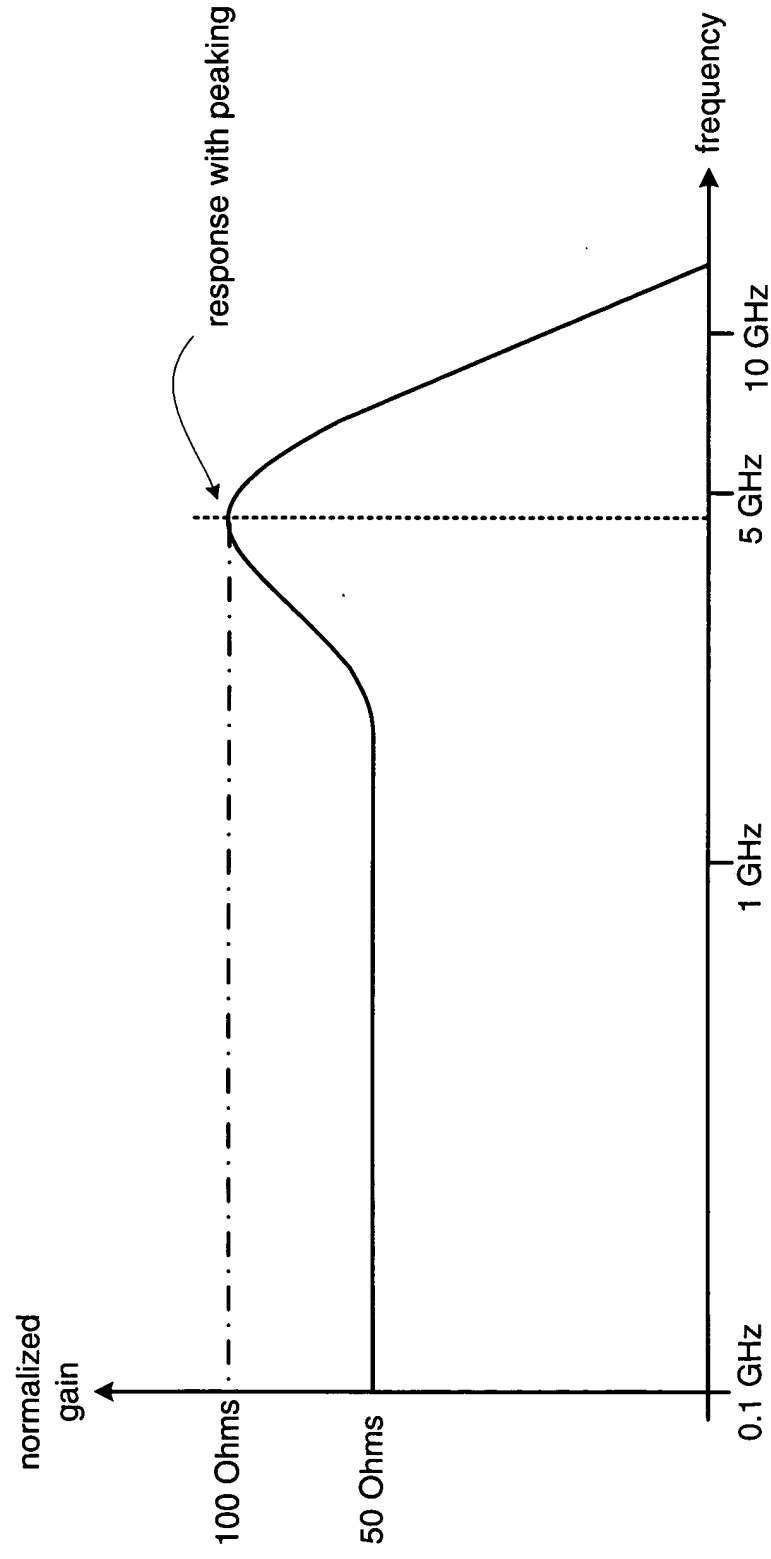


FIG. 8
peaked load stage frequency response

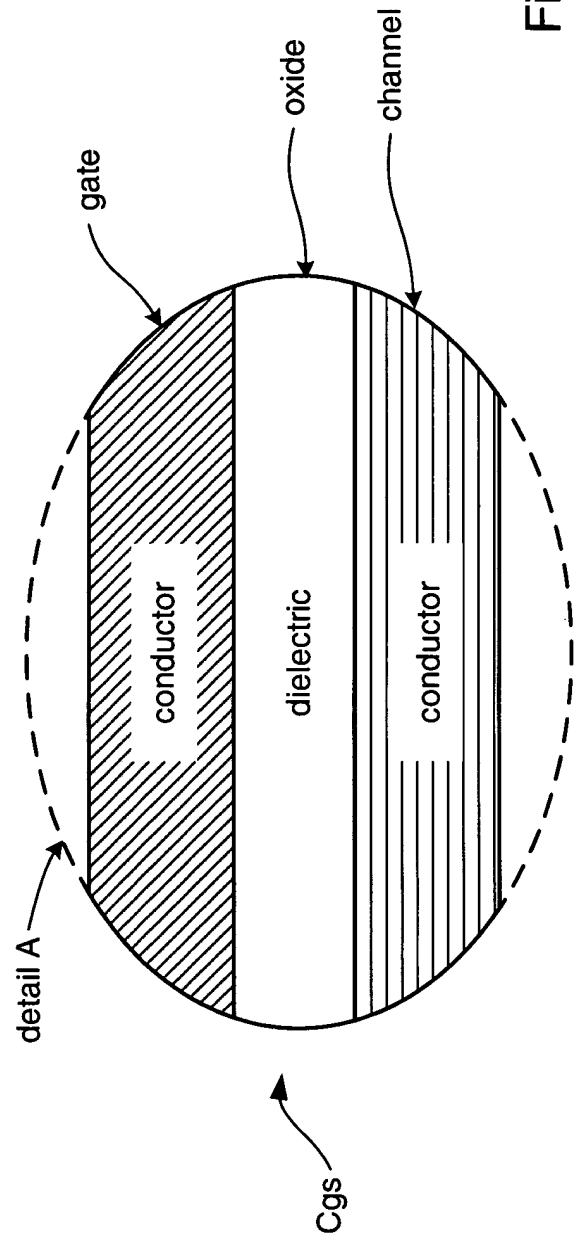
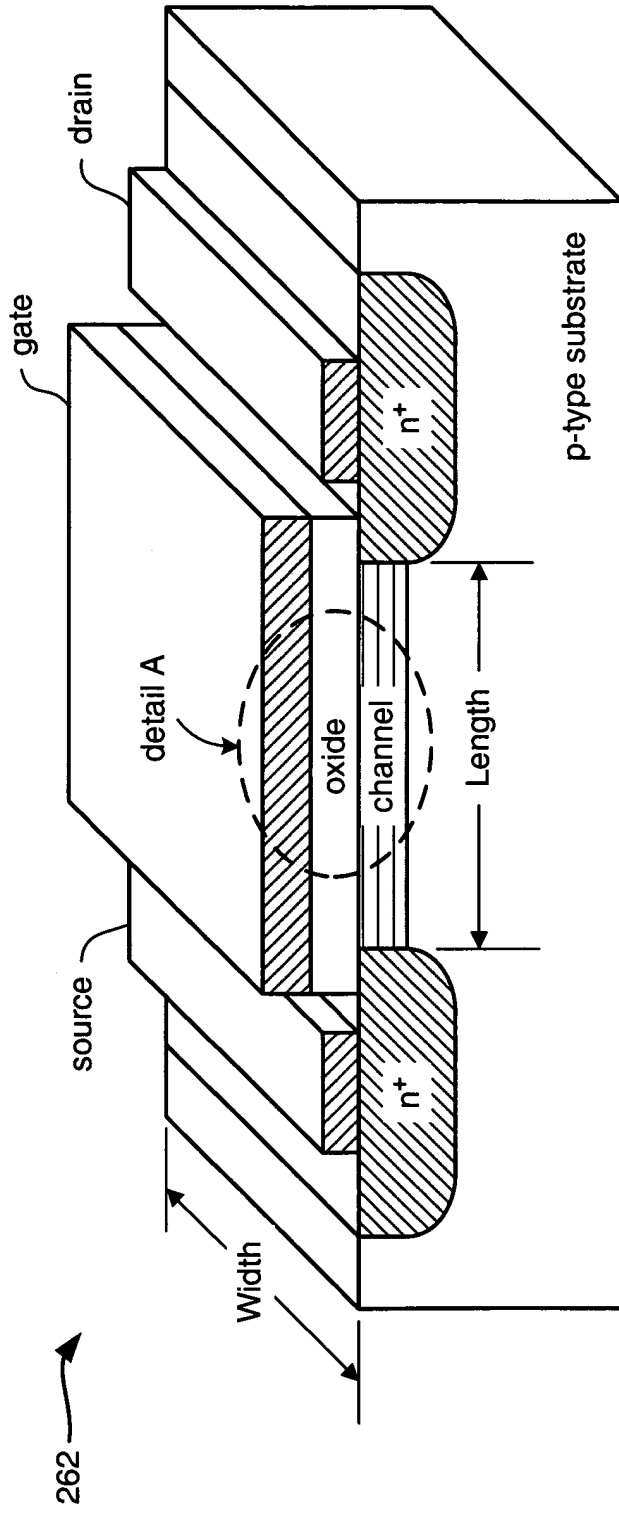


Fig. 9
gate-to-source capacitance

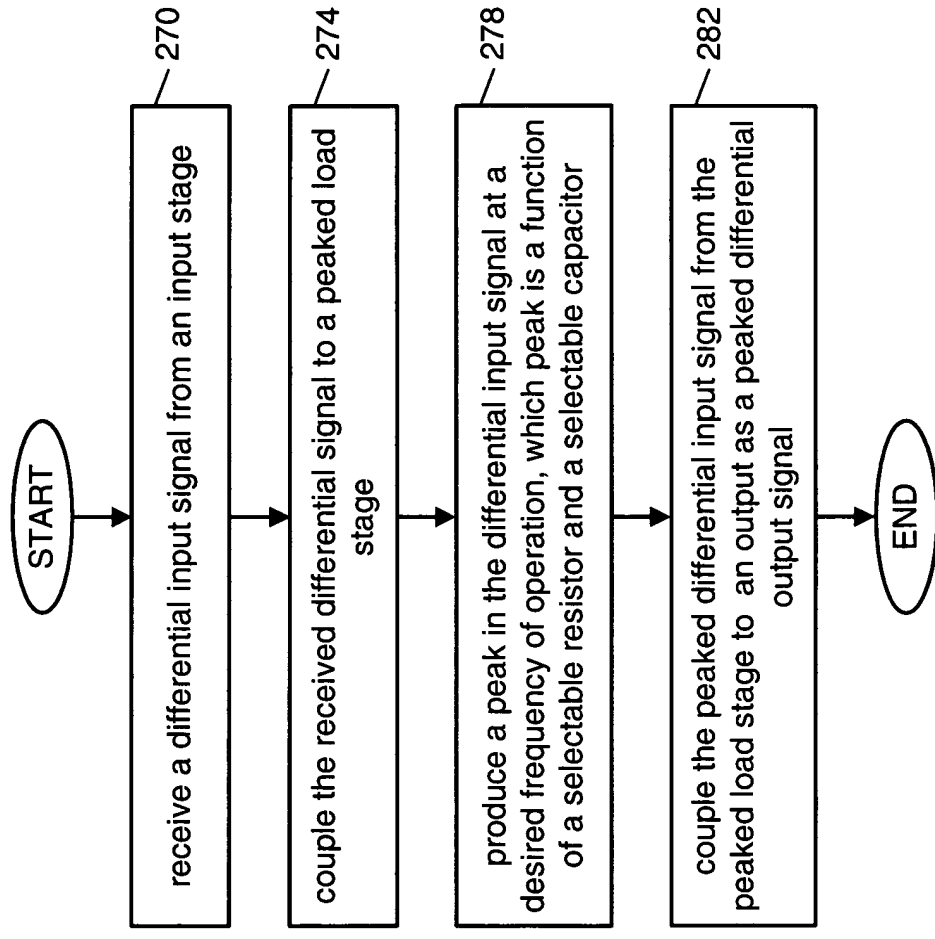


Fig. 10
peaked load method